Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1 and 5 have been amended.

In item 4 of the above-identified Office Action, claims 1 - 6 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,249,893 to Rajsuman et al ("**RAJSUMAN**") in view of U. S. Patent No. 6,320,804 to Dähn ("**DÄHN**"). In item 5 of the above-identified Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **RAJSUMAN** and **DÄHN**, further in view of U. S. Patent Application Publication No. 2002/0055065 to Suzuki et al ("**SUZUKI**"). In item 6 of the above-identified Office Action, claim 8 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **RAJSUMAN** and **DÄHN**, further in view of U. S. Patent No. 5,894,425 to Saliba ("**SALIBA**").

Applicants respectfully traverse the above rejections.

More particularly, Applicants' presently claimed invention requires, among other things, an integrated module including an external access terminal, a memory for storing code and data, and a microcontroller connected to the external access terminal and to the memory. The **microcontroller** of

Applicants' claimed invention, under normal operation, **controls**, among other things, an access to the memory and a data transfer through the external access terminal. The **same microcontroller**, in Applicants' claimed invention, **further controls the performance of a test sequence for functional testing of the memory in a test operation** of the module. In Applicants' invention, a command sequence, on the basis of which the microcontroller controls the carrying out of a test sequence, is read into the module externally before the beginning of the test operation. The loaded command sequence is executed for carrying out the test sequence by the microcontroller.

Further, Applicants' claimed invention requires, among other limitations, a defect data memory for storing/storing of defect data, such as addresses of memory cells of the memory, which have been detected as defective under the control of the microcontroller. For example, Applicants' amended claim 1 recites, among other limitations:

> a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, **said addresses being stored in said defect data memory under control of said microcontroller**. [emphasis added by Applicants]

Similarly, Applicants' independent claim 5 has been amended to recite, among other limitations:

> storing addresses of memory cells of the memory which have been detected as defective during the functional testing in a defect data memory, **said addresses being stored in said defect data memory under control of said microcontroller**. [emphasis added by Applicants]

As such, Applicants' amended independent claims require, among other things, **that the addresses of the memory cells which have been detected as defective are stored in the defect data memory under the control of the microcontroller located on the module and which is used under normal conditions**. The above limitation of Applicants' claims is described in the specification of the instant application, for example, on page 5 of the instant application, lines 15 - 22, which states:

> According to the invention, **the microcontroller, which is provided anyway for the normal operation in the application,** is configured in such a way that, in a test operation of the module, it can control the carrying out of a test sequence for the functional testing of the memory. **Also present is a defect data memory for storing defect data under the control of the microcontroller, the defect data being generated during the checking of functionality.** [emphasis added by Applicants]

At least one advantage to Applicants' claimed invention, is disclosed on page 6 of the instant application, lines 8 - 19, which state:

> The present invention advantageously makes it possible to dispense with BIST hardware on the module. As a result, valuable chip area can be effectively saved. This is particularly advantageous with regard to modules having a high integration density. **The respective defect data can be read out by an external**

> **test unit at the end of the functional test and may serve in particular as a basis for constructing a fail bit map.** As a result, it is possible to use a comparatively cost-effective test system for the functional test since the data communication between the module and the test system does not have to be effected continuously during the test and, therefore, is not time-critical. [emphasis added by Applicants]

However, none of the cited references teach or suggest, among other limitations of Applicants' claims, **defect data memory for storing/storing, under the control of the module's regular microcontroller** (i.e., the microcontroller used by the module under normal operations), **addresses of the memory cells determined to be defective.**

More particularly, the **RAJSUMAN** reference is directed to a method and structure for testing embedded cores in a system-on-chip (SoC) IC including a microprocessor core, a memory core and one or more function-specific cores. In **RAJSUMAN**, a microprocessor core is first tested, then the computation power of this microprocessor core is utilized to generate a memory test pattern, the test patterns are applied to the embedded memory to be tested and the test response thereof is evaluated to determine a fault. See, for example, the Abstract of **RAJSUMAN** and col. 8 of **RAJSUMAN**, lines 41 - 47.

Fig. 9 of **RAJSUMAN** is described, in part, in col. 8 of **RAJSUMAN**, line 51 - col. 9, line 11, which states:

> FIG. 9 is a schematic block diagram showing a structure for testing a memory core 3 by using the embedded microprocessor core 10 whose integrity has been verified. In FIG. 9, a host computer 61, a hard disk 63 and an I/O interface 62 are provided outside of the SoC IC 1. Typically, the hard disk 63 stores the test program to be used in testing the memory core 3. **The host computer 61 provides the executable code of assembly language test program to the microprocessor core 10 in the SoC chip 1 through the I/O interface 62**. A conventional IC tester can also be used to provide the test program to the microprocessor core 10 and to store the test results. However, such a tester may not be necessary and any other means can be used as long as the assembly language test program can be sent to the microprocessor core 10.
>
> **The assembly language test program is converted into binary form by the assembler of the microprocessor core 10**. This assembler may reside in the host computer or the tester, outside the SoC. **Thus, the microprocessor core 10 generates a test pattern from the object code. These test patterns are applied to the memory core 3. According to the algorithm of the test pattern, write data is written in the specified addresses of the memory core 3. The microprocessor core 10 reads the stored data in the memory core 3 to compare the same with the original test data prepared by the microprocessor core 10, which is typically the write data. When the data read from the memory core 3 does not match the expected data, failure information is sent to the host computer 61.** [emphasis added by Applicants]

As can be seen from the foregoing, in **RAJSUMAN**, the microprocessor core 10 just reads the stored data in the memory core 3 to compare the same with original test data prepared by the microprocessor core 10. In **RAJSUMAN**, when the data read from the memory core 3 of **RAJSUMAN does not match the expected data, a "failure information" is sent to the host computer 61 of RAJSUMAN**.

As such, contrary to Applicants' currently claimed invention, **RAJSUMAN** fails to teach or suggest, among other limitations of Applicants' claims, **defect data memory for storing/storing, under the control of module's regular microcontroller** (i.e., the microcontroller used by the module under normal operations), **addresses of the memory cells determined to be defective**. Rather, in **RAJSUMAN**, the microprocessor 10 does not write defect data to a defect data memory (i.e., **RAJSUMAN** discloses "**When the data read from the memory core 3 does not match the expected data, failure information is sent to the host computer 61**").

Further, **RAJSUMAN** also fails to teach or suggest the storing of addresses of faulty memory cells **under the control of the module's regular microcontroller** (i.e., the microcontroller used by the module under normal operations). Rather, col. 9 of **RAJSUMAN**, lines 23 - 26, state:

> It should also be noted that the test program as shown in the foregoing may stop as soon as an error occurs. **The host computer or IC tester immediately observes the failure and hence, fail-bit location is immediately known.** [emphasis added by Applicants]

As such, the microprocessor of the module under test, in **RAJSUMAN** does not even make note of the fail-bit "location".

The failure of **RAJSUMAN** to even store **addresses** of memory

cells determined to be detected is additionally supported by page 4 of the Office Action, which states, in part:

> Rajsuman et al. mention that the user can modify the test program to collect any desired test information of the embedded memory (col. 9 lines 25 - 28) **but does not explicitly teach the storing addresses of the memory cells of said memory which have been detected as defective.** [emphasis added by Applicants]

Rather, page 4 of the Office Action goes on to state, in part:

> Dahn disclosed the memory unit for storing addresses of defective memory cells (fig. 2, 10, col. 5 lines 6 - 15).
>
> It would have been obvious to modify the module of Rajsuman et al. by adding Dahn memory unit for storing addresses of defective memory cells. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would have considerable time advantage in the subsequent redundancy analysis (col. 3, lines 34 - 41).

Applicants believe that the **DÄHN** reference, like the **RAJSUMAN** reference, fails to teach or suggest, among other limitations of Applicants' claimed invention, **defect data memory for storing/storing, under the control of the module's regular microcontroller** (i.e., the microcontroller used by the module under normal operations), **addresses of the memory cells determined to be defective.**

More particularly, **DÄHN** discloses an integrated semiconductor memory with a memory unit for storing addresses of defective

memory cells. Col. 1 of **DÄHN**, lines 51 - 55, state:

> Since memory cells are subjected to a number of tests, if a particular test is not passed, it must be determined whether the defect address has already been stored because of a failure of a previous test. This determination must be performed before the address of the defective memory cell is stored. If this is the case, the defect address should not be stored a second time, in order to save memory space. **The defect addresses may be stored in a separate memory cell array on the chip to be tested. This additional memory cell array is then part of, for example, a self-testing device of the memory chip.** [emphasis added by Applicants]

As such, **DÄHN** does **not** disclose **a microprocessor** configured to determine addresses of defective memory cells and to store the determined addresses in a defect data memory. Rather, according to the **DÄHN** reference, testing systems that use a so-called fail address memory (FAM), store the addresses of defective memory cells in a defect data memory arranged **in a separate memory cell array on the chip which is part of a self-testing device of the memory chip**. See, for example, col. 4 of **DÄHN**, 13 - 16.

Further, **DÄHN** discloses **a preprocessing device** (3 of Fig. 2 of **DÄHN**), having memory devices 4 and 5, **for storing a fixed number of addresses of defective normal memory cells.** However, contrary to Applicants' claimed invention (i.e., wherein, the microcontroller used for normal also controls the storage of addresses of faulty memory cells in a defect data

memory), **DÄHN** discloses the **storage** of the fixed number of addresses of defective normal memory cells **being controlled by control signals for controlling generated by a self-testing (BIST) unit**. See, for example, col. 4 of **DÄHN**, line 54 - col. 5, line 5, which states:

> The preprocessing device 3 has memory devices 4 and 5 for storing a fixed number of addresses of defective normal memory cells MC. Each of the memory devices 4 and 5 has register units 6 for respectively storing one of the address parts ADR 1 or ADR2. The register units 6 are connected to each other in the form of a shift register. Outputs 61 of the register units 6 are connected to inputs 71 of a comparison device 7. The output 72 of the comparison device 7 is connected to the output 31 of the preprocessing device 3 via the control 9. A comparison device 8 is connected in a way analogous to the comparison device 7 to corresponding outputs of the memory device 5 and via the control 9 to the output 31 of the preprocessing device 3. A signal 91 of the control 9 serves for switching over between the signals 92 and 93 as the input signal of the control 9. The clock signal clk and **the signal F, which is generated for example by a self-testing unit, serve as control signals for controlling the storing operation of the memory devices 4 and 5 and as input signals of the control 9.** [emphasis added by Applicants]

As such, in **DÄHN**, a self-testing unit controls the storage of defect addresses, which is contrary to Applicants' currently claimed invention requiring **the microcontroller used for normal operation to store addresses of faulty memory cells in the defect data memory.**

In view of the foregoing, it can be seen that both, **RAJSUMAN** and **DÄHN**, fail to teach or suggest, among other limitations of

Applicants' claims, defect data memory for storing/storing, **under the control of the module's regular microcontroller** (i.e., the microcontroller used by the module under normal operations), addresses of the memory cells determined to be defective. As such, Applicants' claims are believed to be patentable over **RAJSUMAN** and **DÄHN**, whether taken alone, or in combination.

Additionally, the **SUZUKI** and **SALIBA** references, cited in the Office Action in combination with **RAJSUMAN** and **DÄHN** against certain of Applicants' dependent claims, fail to cure the above-discussed deficiencies of the **RAJSUMAN** and **DÄHN** references.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5.

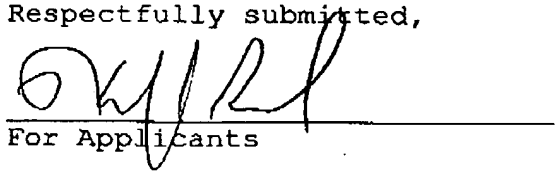
In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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